NTHD4102P

Power MOSFET

−20 V, −4.1 A, Dual P−Channel ChipFET™

Features

- Offers an Ultra Low $R_{DS(ON)}$ Solution in the ChipFET Package
- Miniature ChipFET Package 40% Smaller Footprint than TSOP−6
- Low Profile (<1.1 mm) Allows it to Fit Easily into Extremely Thin Environments such as Portable Electronics
- Simplifies Circuit Design since Additional Boost Circuits for Gate Voltages are not Required
- Operated at Standard Logic Level Gate Drive, Facilitating Future Migration to Lower Levels using the same Basic Topology
- Pb−Free Package is Available

Applications

- Optimized for Battery and Load Management Applications in Portable Equipment such as MP3 Players, Cell Phones, and PDAs
- Charge Control in Battery Chargers
- Buck and Boost Converters

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	−20	V
Gate−to−Source Voltage			V_{GS}	±8.0	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	−2.9	A
		T_A = 85°C		−2.1	
	t ≤ 10 s	T_A = 25°C		−4.1	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	1.1	W
	t ≤ 10 s			2.1	
Pulsed Drain Current	tp = 10 ms		I_{DM}	−13.8	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode)			I_S	−1.1	A
Lead Temperature for Soldering Purposes (1/8” from case for 10 s)			T_L	260	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Ambient, Steady State (Note 1)	$R_{\theta JA}$	113	°C/W
Junction−to−Ambient, t ≤ 10s (Note 1)		60	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)

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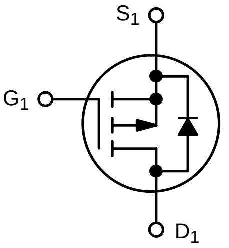
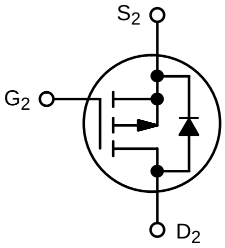
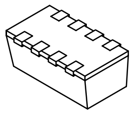
$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	I_D MAX
−20 V	64 mΩ @ −4.5 V	−4.1 A
	85 mΩ @ −2.5 V	
	120 mΩ @ −1.8 V	



P−Channel MOSFET

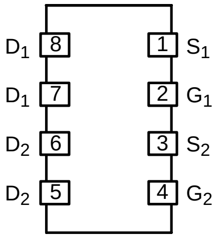


P−Channel MOSFET

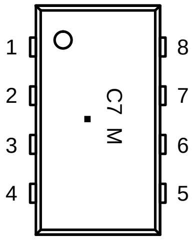


ChipFET
CASE 1206A
STYLE 2

PIN CONNECTIONS



MARKING DIAGRAM



C7 = Specific Device Code
M = Month Code
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTHD4102PT1	ChipFET	3000/Tape & Reel
NTHD4102PT1G	ChipFET (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(Br)DSS}$	V_{GS} = 0 V, I_D = −250 μA		−20			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(Br)DSS}/T_J$				−15		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V V_{DS} = −16 V	T_J = 25°C			−1.0	μA
			T_J = 85°C			−5.0	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8.0 V				±100	nA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA		−0.45		−1.5	V
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				2.7		mV/°C
Drain−to−Source On Resistance	$R_{DS(ON)}$	V_{GS} = −4.5 V, I_D = −2.9 A			64	80	mΩ
		V_{GS} = −2.5 V, I_D = −2.2 A			85	110	
		V_{DS} = −1.8 V, I_D = −1.0 A			120	170	
Forward Transconductance	g_{FS}	V_{DS} = −10 V, I_D = −2.9 A			7.0		S
CHARGES, CAPACITANCES, AND GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = −16 V			750		pF
Output Capacitance	C_{OSS}				100		
Reverse Transfer Capacitance	C_{RSS}				45		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −4.5 V, V_{DS} = −16 V, I_D = −2.6 A			7.6	8.6	nC
Gate−to−Source Charge	Q_{GS}				1.3		
Gate−to−Drain Charge	Q_{GD}				2.6		
SWITCHING CHARACTERISTICS (Note 3)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = −4.5 V, V_{DD} = −16 V, I_D = −2.6 A, R_G = 2.0 Ω			5.5	10	ns
Rise Time	t_r				12	25	
Turn−Off Delay Time	$t_{d(OFF)}$				32	40	
Fall Time	t_f				23	35	
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −1.1 A			−0.8	−1.2	V
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 1.0 A			20	40	ns
Charge Time	ta				15		
Discharge Time	tb				5		
Reverse Recovery Charge	Q_{RR}				0.01		μC

2. Pulse test: pulse width ≤ 300 μs, duty cycle ≤ 2%
3. Switching characteristics are independent of operating junction temperatures

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

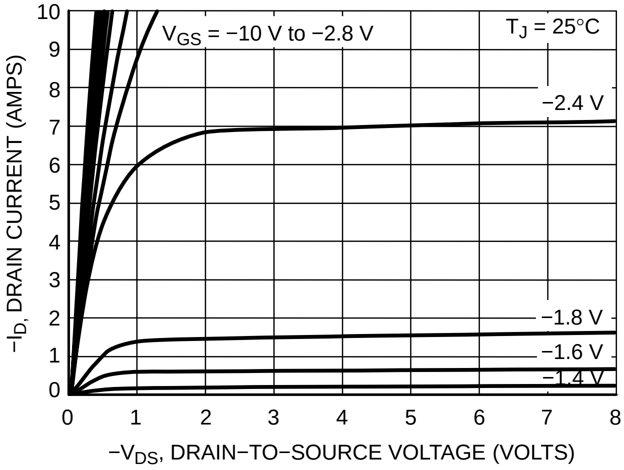


Figure 1. On−Region Characteristics

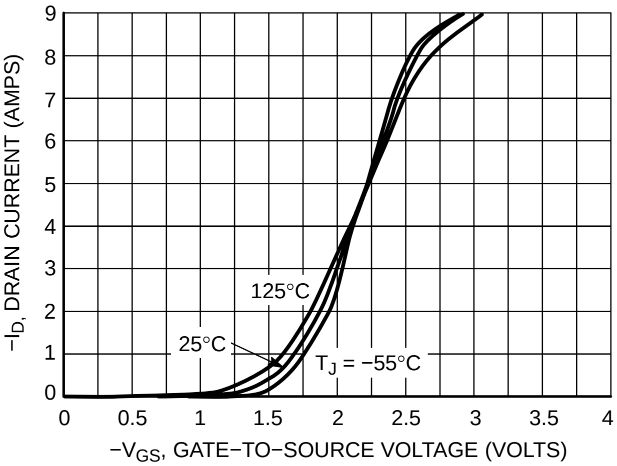


Figure 2. Transfer Characteristics

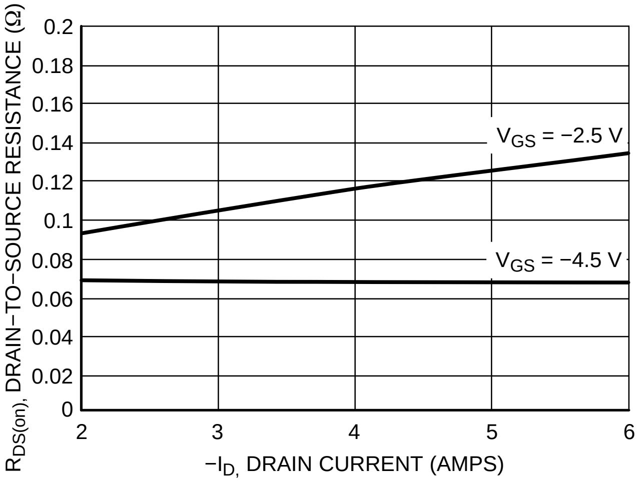


Figure 3. On−Resistance vs. Drain Current and Gate Voltage

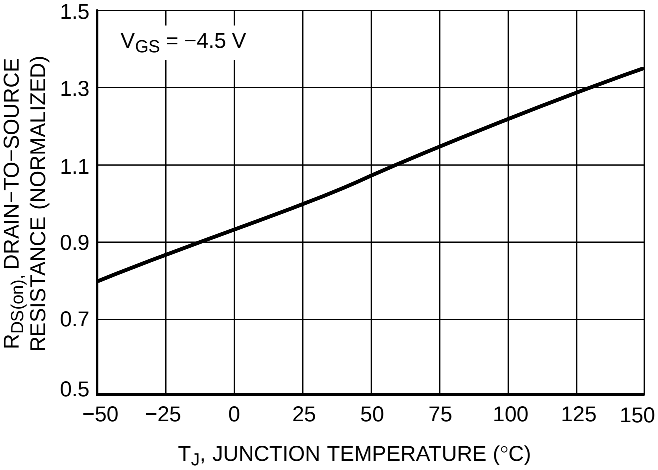


Figure 4. On−Resistance Variation with Temperature

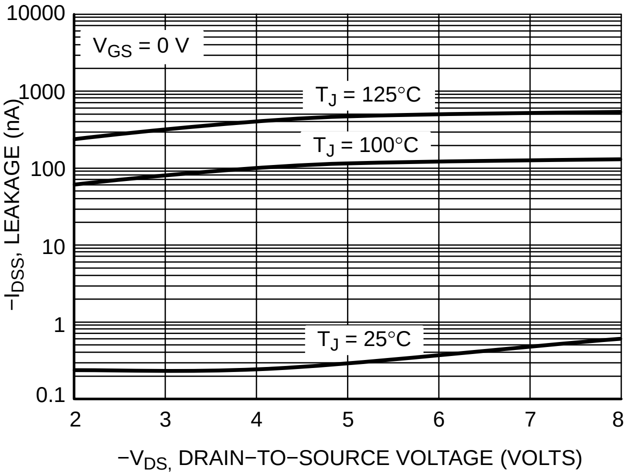


Figure 5. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

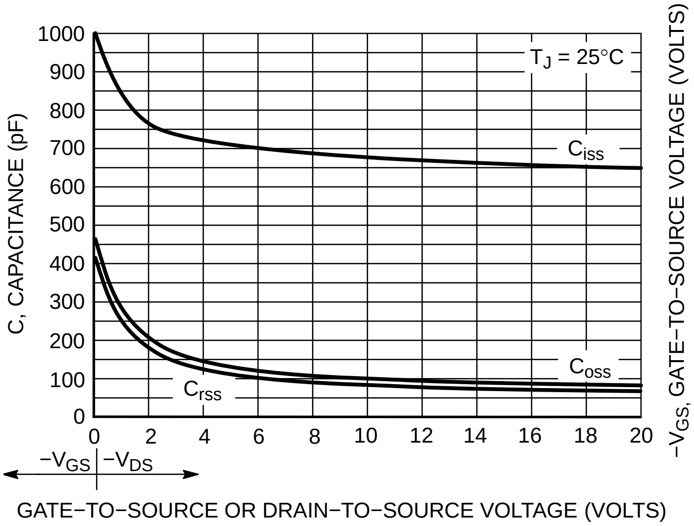


Figure 6. Capacitance Variation

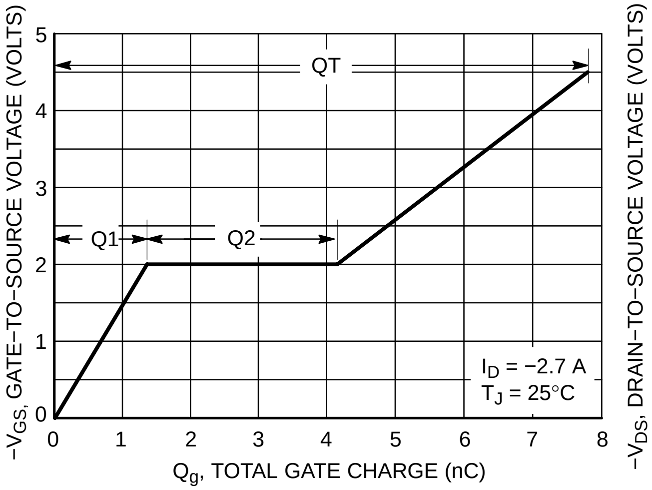


Figure 7. Gate−to−Source and Drain−to−Source Voltage vs. Total Gate Charge

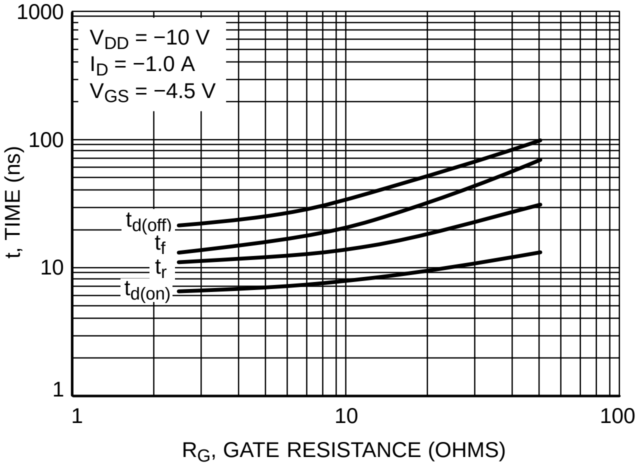


Figure 8. Resistive Switching Time Variation vs. Gate Resistance

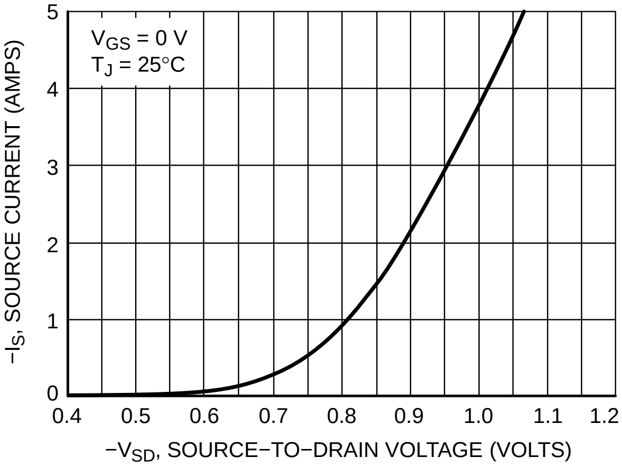


Figure 9. Diode Forward Voltage vs. Current

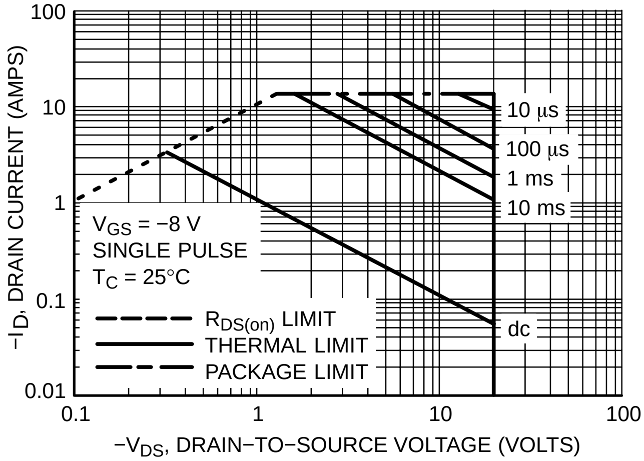
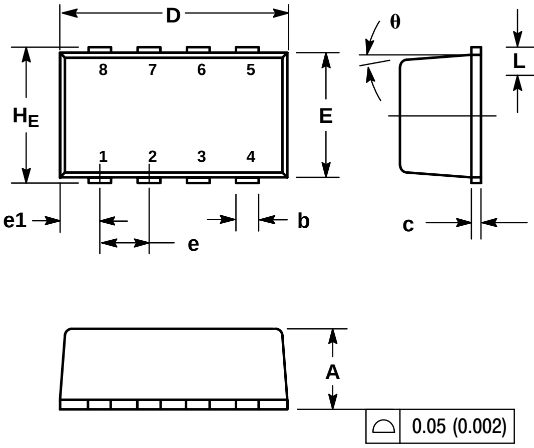


Figure 10. Maximum Rated Forward Biased Safe Operating Area

PACKAGE DIMENSIONS

ChipFET™
CASE 1206A−03
ISSUE G

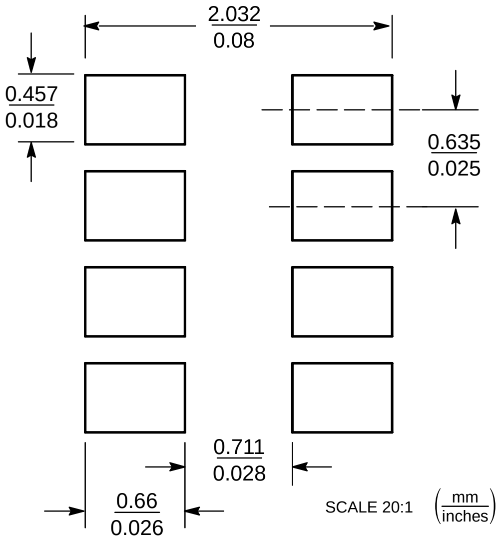


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

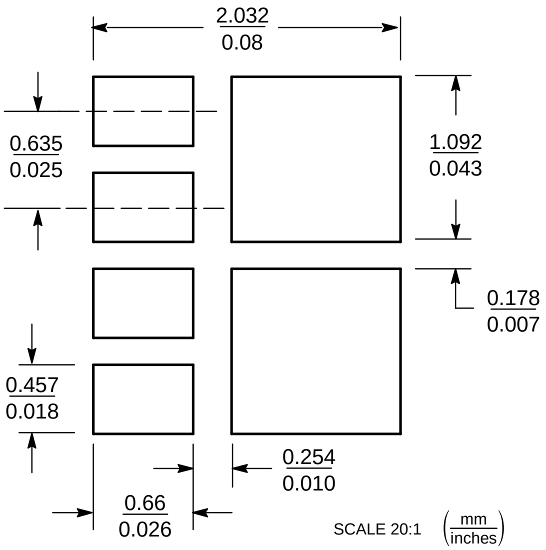
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
H_E	1.80	1.90	2.00	0.071	0.075	0.079
θ	5° NOM			5° NOM		

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

SOLDERING FOOTPRINT*



Basic



Style 2

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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